

VIPER (VME Interfaced to PCI EXODET Readout): general purpose front-end electronics and DAQ for nuclear physics experiments with highly segmented detectors

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I. INTRODUCTION

The usage of highly segmented detectors is a mandatory task in the modern detector arrays for nuclear physics experiments. The requirements of a high position resolution and solid angle coverage along with the necessity to keep the costs to an accessible level have brought us to design and build a new experimental apparatus named EXODET [1]. The basic element of EXODET is a large area silicon SSD, single side segmented in 100 strips. The full setup consists of 8 two-stage telescopes, which amounts to a total of 1600 strips. To perform the readout from such a segmented detector unit we have developed several new front-end electronic boards, one of which employs a high integration ASIC chipset, the AToM chip [2]. The new front-end electronics is interfaced to the VME bus. A new data acquisition system, named **VIPER** (VME Interfaced to PCI EXODET Readout), has been designed from scratch to manage the readout from homemade and commercial electronic modules. We decided to base the new developments on the VME bus because of its widespread use in nuclear physics laboratories and for the large variety of front-end modules (ADC, TDC, QDC, scalers...) commercially available.

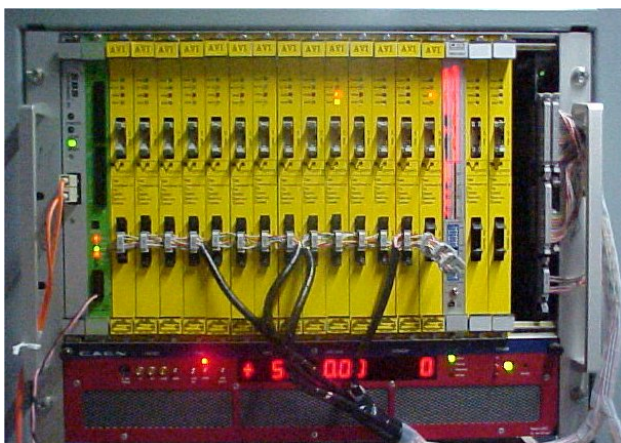


FIG. 1: The VIPER front-end VME crate containing, from left to right, the VME-PCI bridge board (gray), a commercial 32 channel ADC (green), 16 AVI boards (yellow) and the TSI board.

The new electronic boards have been entirely designed and built by the **S.E.R.** (Servizio Elettronica e Rivelatori) of the INFN, Sezione di Napoli.

In short, the main guidelines of the VIPER DAQ design have been:

- easy integration of homemade electronics with standard commercial ones;
- possibility of low cost upgrading;
- expandability towards multiprocessor and multi-node configurations;
- utilization of network distributed resources;
- reduced CPU obsolescence problems;
- flexible software architecture to simplify module setup and on-line monitoring;
- high transportability of the system to different laboratories.

II. FRONT-END ELECTRONICS

FIG.1 shows a picture of the front-end VME crate used in VIPER, and FIG.2 shows a schematic diagram of the electronic readout chain. The hardware/software components developed in this project are shown in orange. The silicon detector is mounted on an interface board that also contains the AToM chip. This board is interfaced to the VME bus through the AVI board (AToM to VME Interface). There is one AVI board per chip and in a forthcoming project one board will be capable of managing 8 AToM chips. The TSI board (Trigger Supervisor Interface) is a highly versatile board and is the trigger supervisor of the whole front-end (i.e., trigger filter and deliverer). The AVI board manages the communication channels between the chip and the VME bus for operations like sending setup or calibration commands to the chip. When the acquisition is running and the TSI board asserts a valid trigger signal, the AVI sends the trigger command to the chip and makes available to the VME bus the data stream received from the chip. Signals regarding the internal status of the AVI board and/or the chip connected to it are sent, via the control bus, back to the TSI board which, in turn, has also the role of reporting occurrences of errors, FIFO half-full signals, and other important control signals. Another important task performed by the TSI

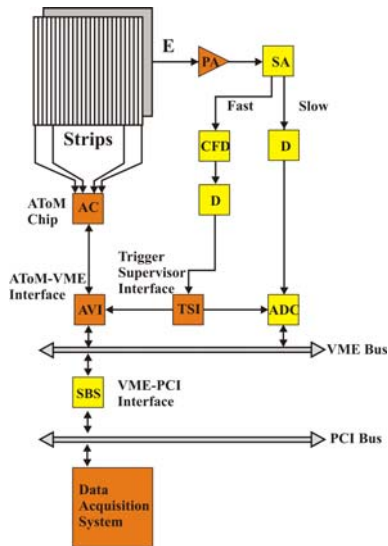


FIG. 2: Scheme of the electronic chain for one of the EXODET detectors. The orange colored boxes represent homemade electronics or software, whereas the yellow ones represent commercial equipments.

board is the logical combination (OR/AND) of all the input channels deputed to provide a trigger signal. When a channel proposes a trigger signal, before promoting it to a valid trigger, the TSI board controls that the whole system is ready (i.e., no AVI is busy, no error occurred, acquisition is running,...). It is possible to mask or sample one or more of the input channels and to force a valid trigger assertion for testing purposes. An external inhibit signal can also be used to integrate commercial boards in the readout system. This is the case for the ADC used to encode the energy signal from the silicon detector: the inhibit signal comes from the ADC, and is kept asserted by the ADC itself until the data digitization cycle has been completed. To evaluate the dead time, the TSI board has been equipped with rate meters and counters for the proposed and accepted triggers. Furthermore, dividers by 10/100/1000 can also be used for the input channels. Finally, the TSI board is also used to synchronize all the front-end boards in order to guarantee a common time stamp.

To ensure a complete reconfiguration of the developed electronics and flexibility with respect to wider experimental requirements, FPGAs have been extensively used in the design of the boards along with advanced techniques to optimize the connection arrangement between them.

The VME bus is connected to a PC via a commercial VME-PCI bridge. This solution reduces the problems due to the CPU obsolescence, allows a progressive low-cost enhancement of the DAQ system performances with the upgrade of the CPUs available on the market, and does not link the DAQ software to a specific platform. The choice of transferring the CPU from the VME bus to the PC also

allows taking the most advantage from of continuous improvement of the I/O devices (disks, RAM, DVD writer...) of the PC industry.

III. DATA ACQUISITION SYSTEM

One of the VIPER DAQ software components has been designed on the basis of a *Producer/Consumer* model: the *Producer* is the readout process and the *Consumers* are processes like event buffering, delivering, storing, and histogramming. Both the architecture and the hierarchy of the processes are suitable for a multiprocessor environment built on a multinode configuration. The whole system, schematically shown in FIG.3, is accessible over the network because of a *Server/Client* architecture. The *Server* is the process that manages the hardware and runs on the PC directly linked to the front-end. The *Clients* operate on the front-end and monitor the data acquisition through the *Server*. The DAQ system can manage more than one VME crate and includes an innovative and general method to setup the front-end modules, and the relative on-line analysis, which eliminates the burden due to the implementation of software drivers for new modules. The user can quickly operate a new module without the need of intervention on the DAQ core software. The whole software has been developed in the C/C++ languages for the Linux operating system platform, and using the OSF/Motif environment for the graphical user interface.

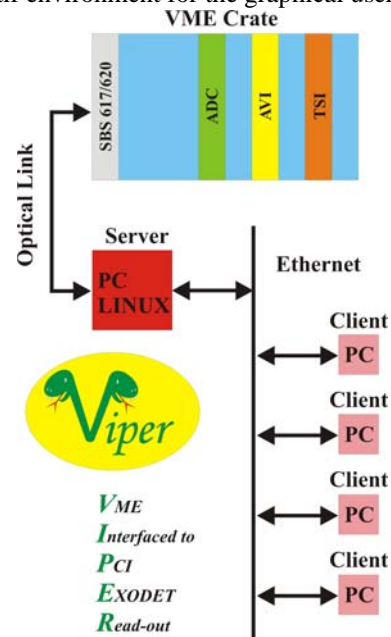


FIG. 3: Schematic drawing of VIPER. The front-end VME crate is linked to a personal computer via a VME-PCI bridge board. The DAQ software runs on a Linux environment and the whole system is accessible over the network.

- [1] M. Romoli et al., "EXODET.....", this Report
 [2] A. Perazzo et al., BABAR Note #501 (1999).